100

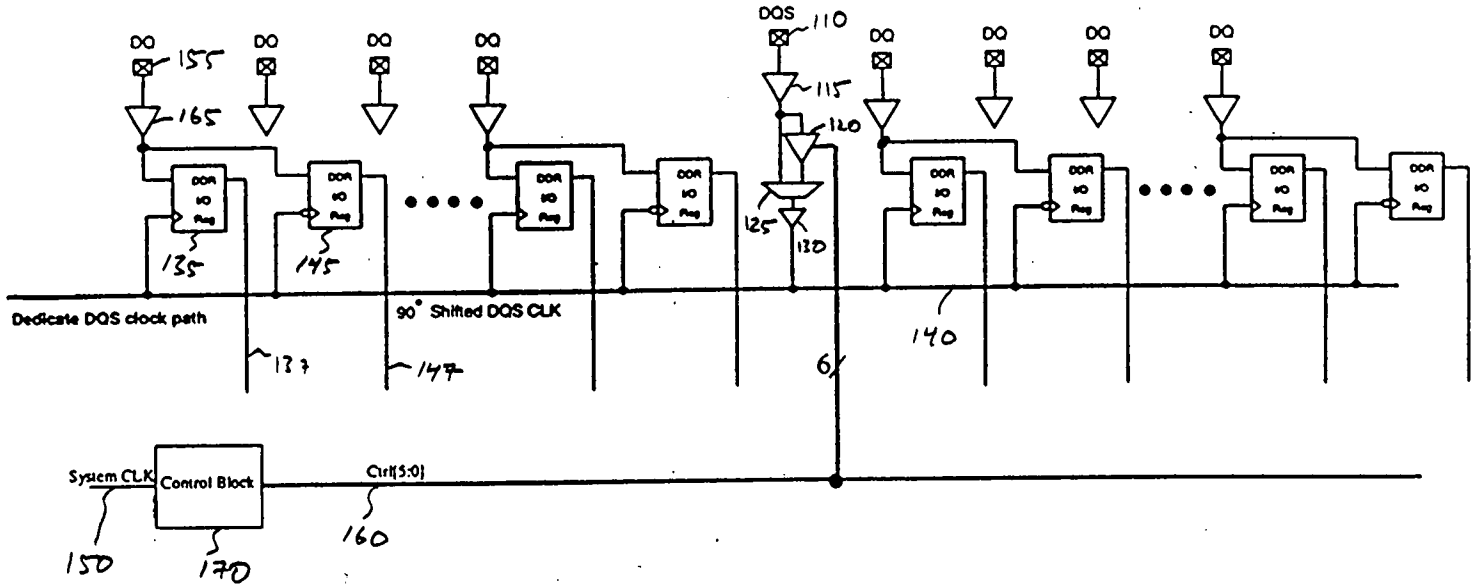
DQS
110
DQ
155
165
115
120
125
130
135
145
140
Dedicate DQS clock path
90° Shifted DQS CLK
127
147
System CLK
Control Block
Ctrl[3:0]
150
170
160

FIGURE 1

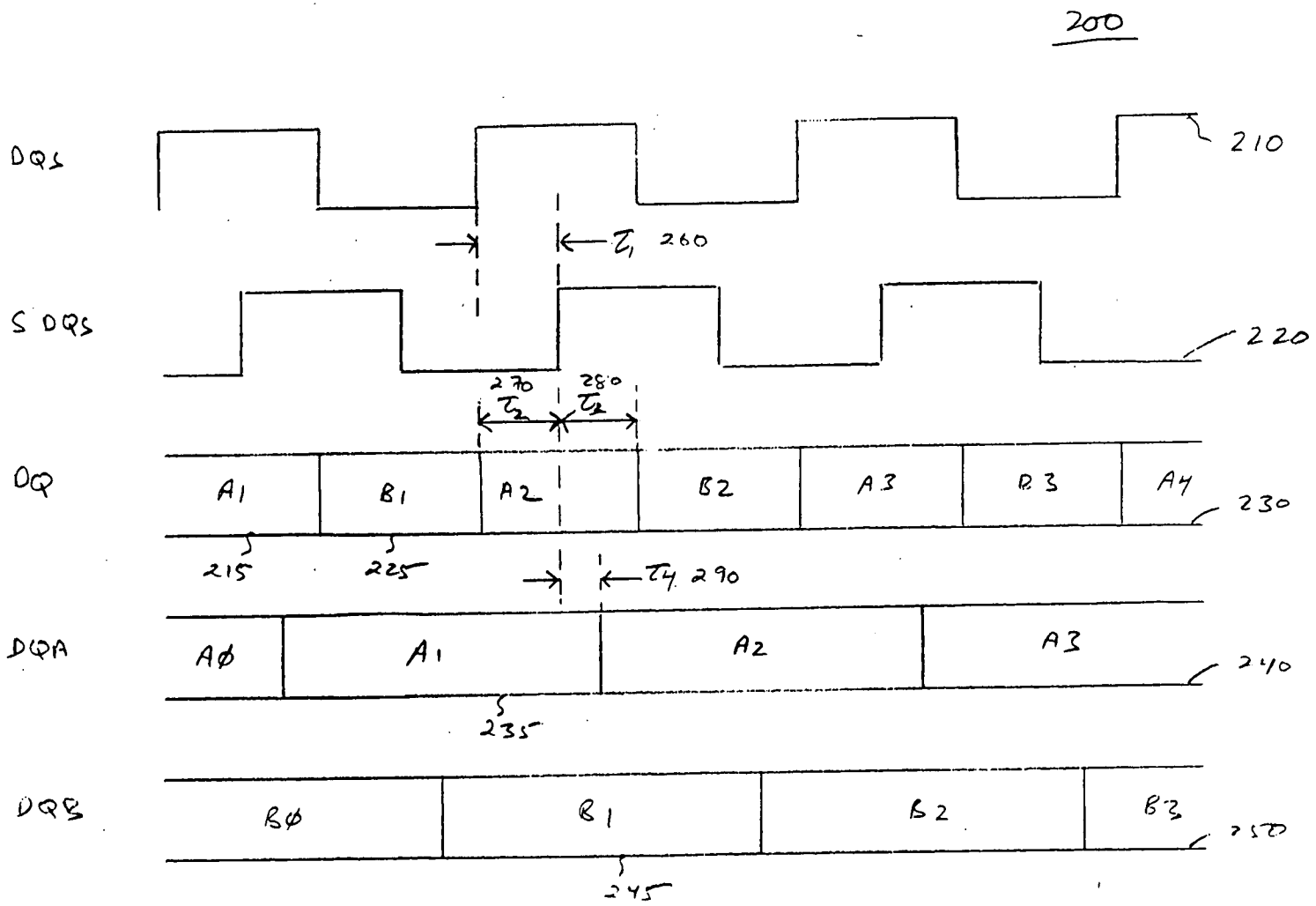
200
DQS
210
T_1 260
S DQS
220
270 T_2
280 T_3
DQ
A1
B1
A2
B2
A3
B3
A4
230
215
225
T_4 290
DQA
Aϕ
A1
A2
A3
240
235
DQB
Bϕ
B1
B2
B3
250
245

FIGURE 2

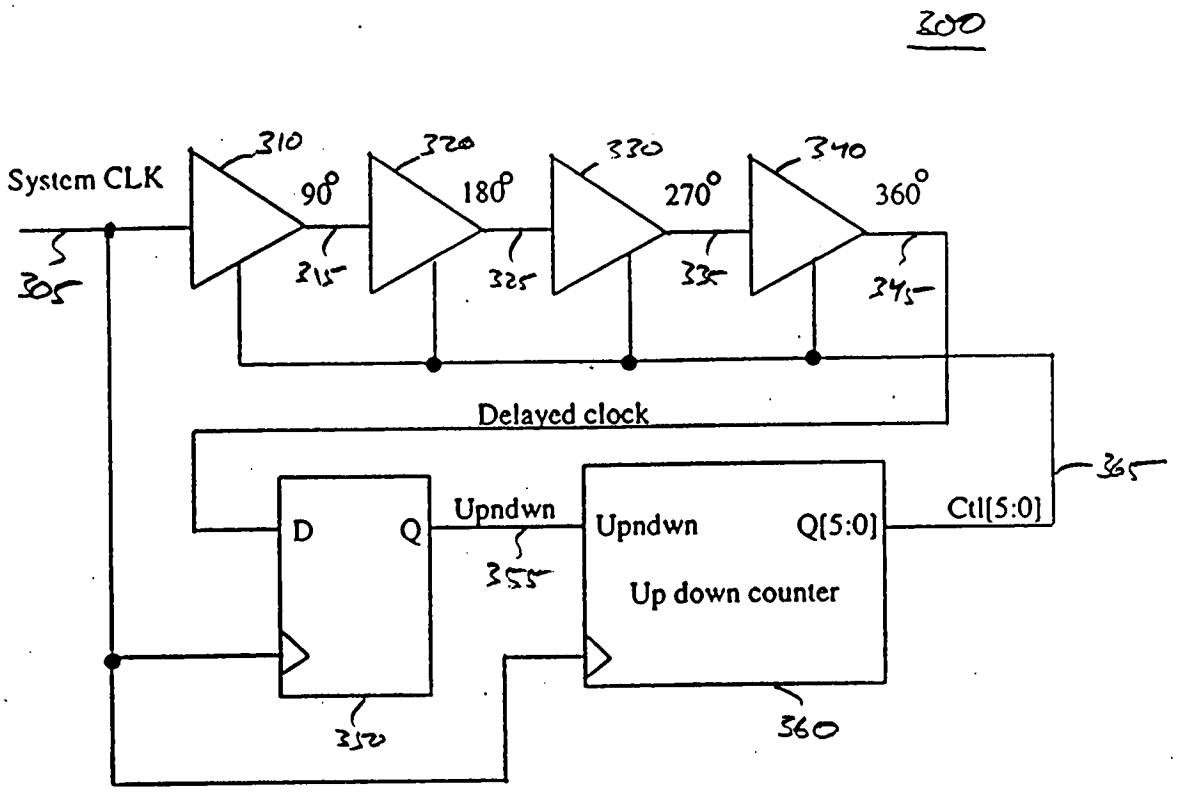
300
System CLK
310
320
330
340
90°
180°
270°
360°
305
315
325
335
345
Delayed clock
365
D
Q
Upndwn
355
Upndwn
Q[5:0]
Ctl[5:0]
Up down counter
350
360

FIGURE 3

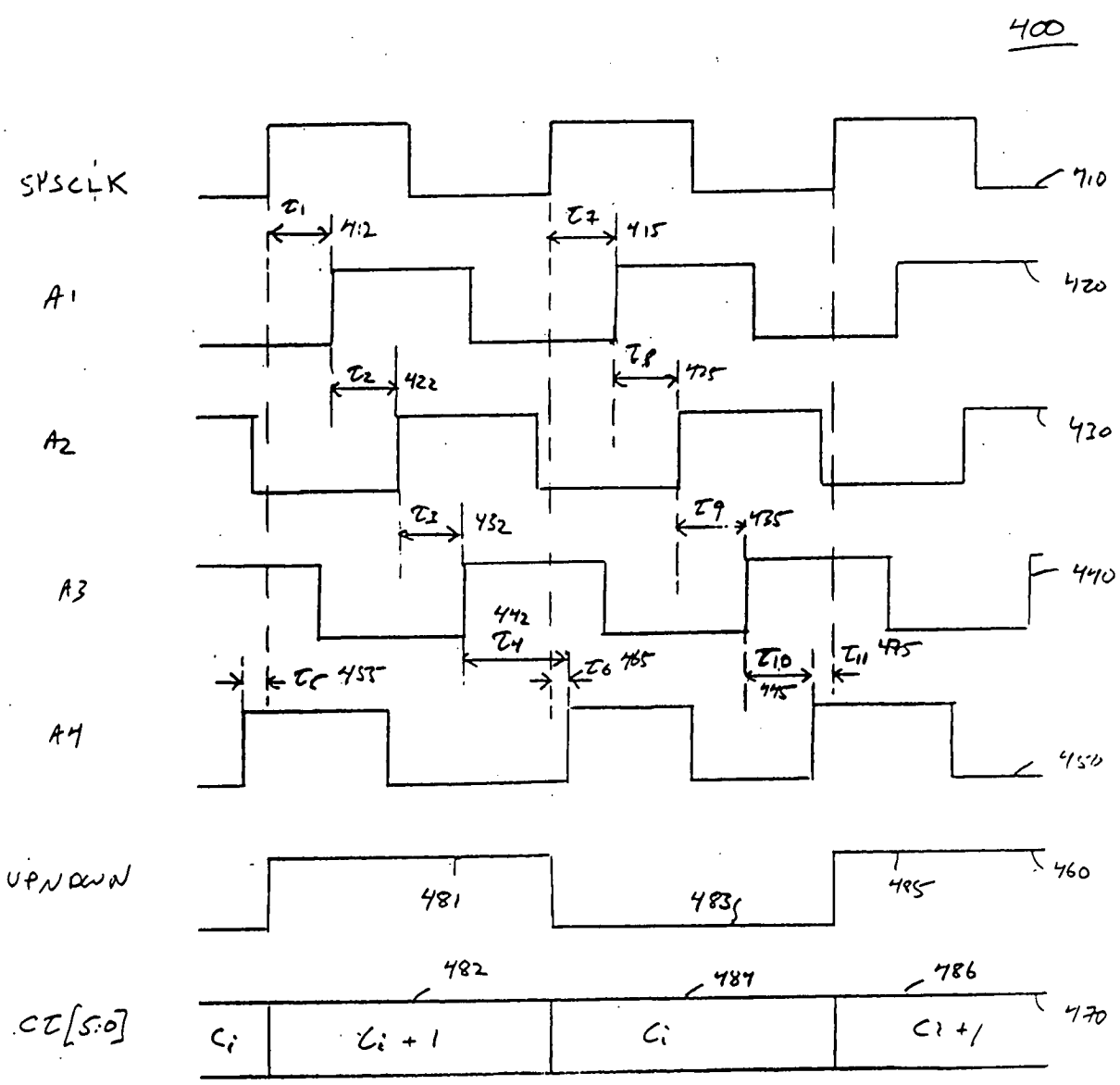
400
SYSCLK
A1
A2
A3
A4
UP/DOWN
CC[5:0]
710
τ1
712
τ7
715
720
τ8
725
τ2
722
730
τ3
732
τ9
735
740
τ4
742
τ6
745
τ5
755
τ10
745
τ11
745
750
760
481
483
485
Ci
Ci + 1
Ci
Ci + 1
770
782
784
786

FIGURE 4

500

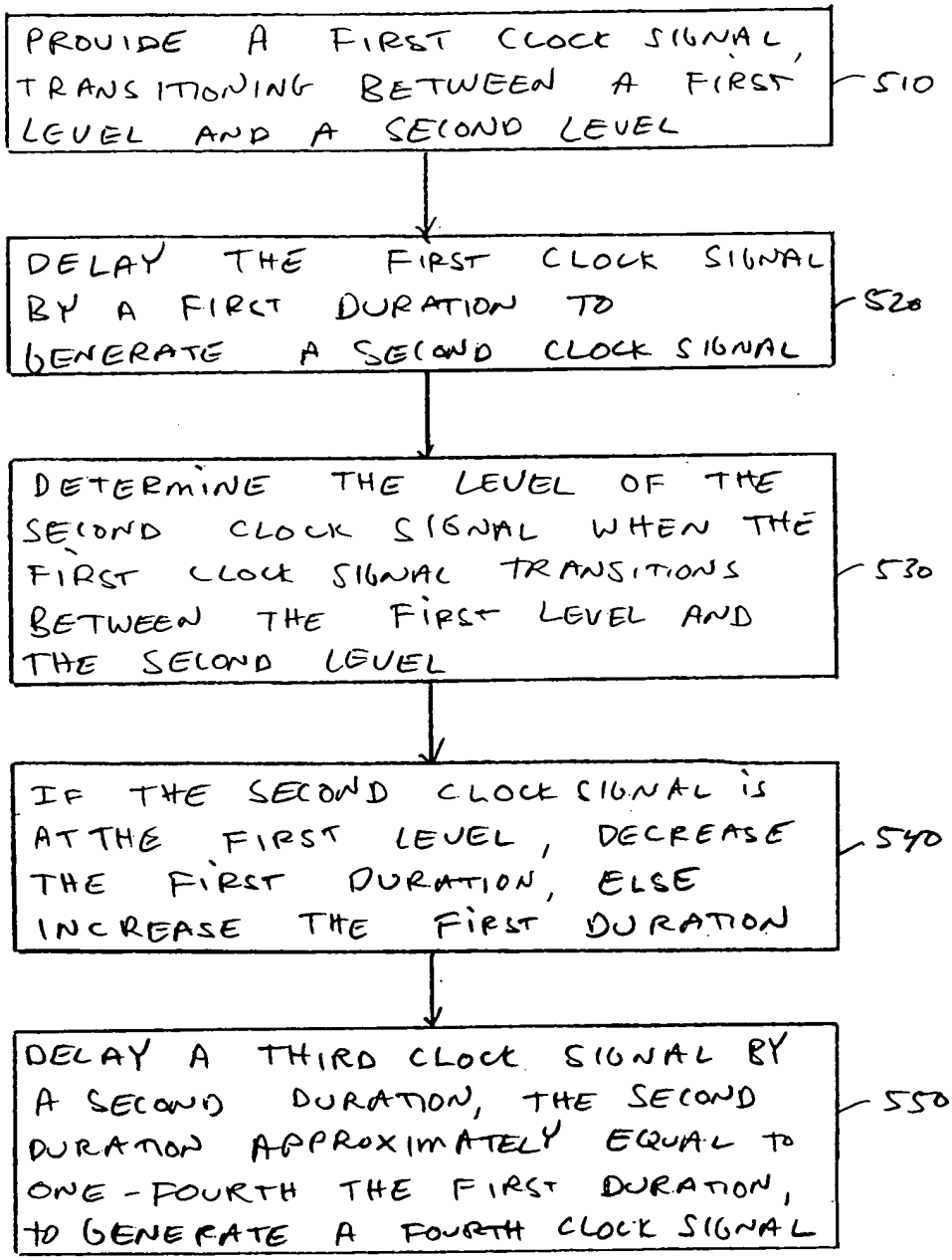
PROVIDE A FIRST CLOCK SIGNAL, TRANSITIONING BETWEEN A FIRST LEVEL AND A SECOND LEVEL
510
DELAY THE FIRST CLOCK SIGNAL BY A FIRST DURATION TO GENERATE A SECOND CLOCK SIGNAL
520
DETERMINE THE LEVEL OF THE SECOND CLOCK SIGNAL WHEN THE FIRST CLOCK SIGNAL TRANSITIONS BETWEEN THE FIRST LEVEL AND THE SECOND LEVEL
530
IF THE SECOND CLOCK SIGNAL IS AT THE FIRST LEVEL, DECREASE THE FIRST DURATION, ELSE INCREASE THE FIRST DURATION
540
DELAY A THIRD CLOCK SIGNAL BY A SECOND DURATION, THE SECOND DURATION APPROXIMATELY EQUAL TO ONE-FOURTH THE FIRST DURATION, TO GENERATE A FOURTH CLOCK SIGNAL
550

FIGURE 5

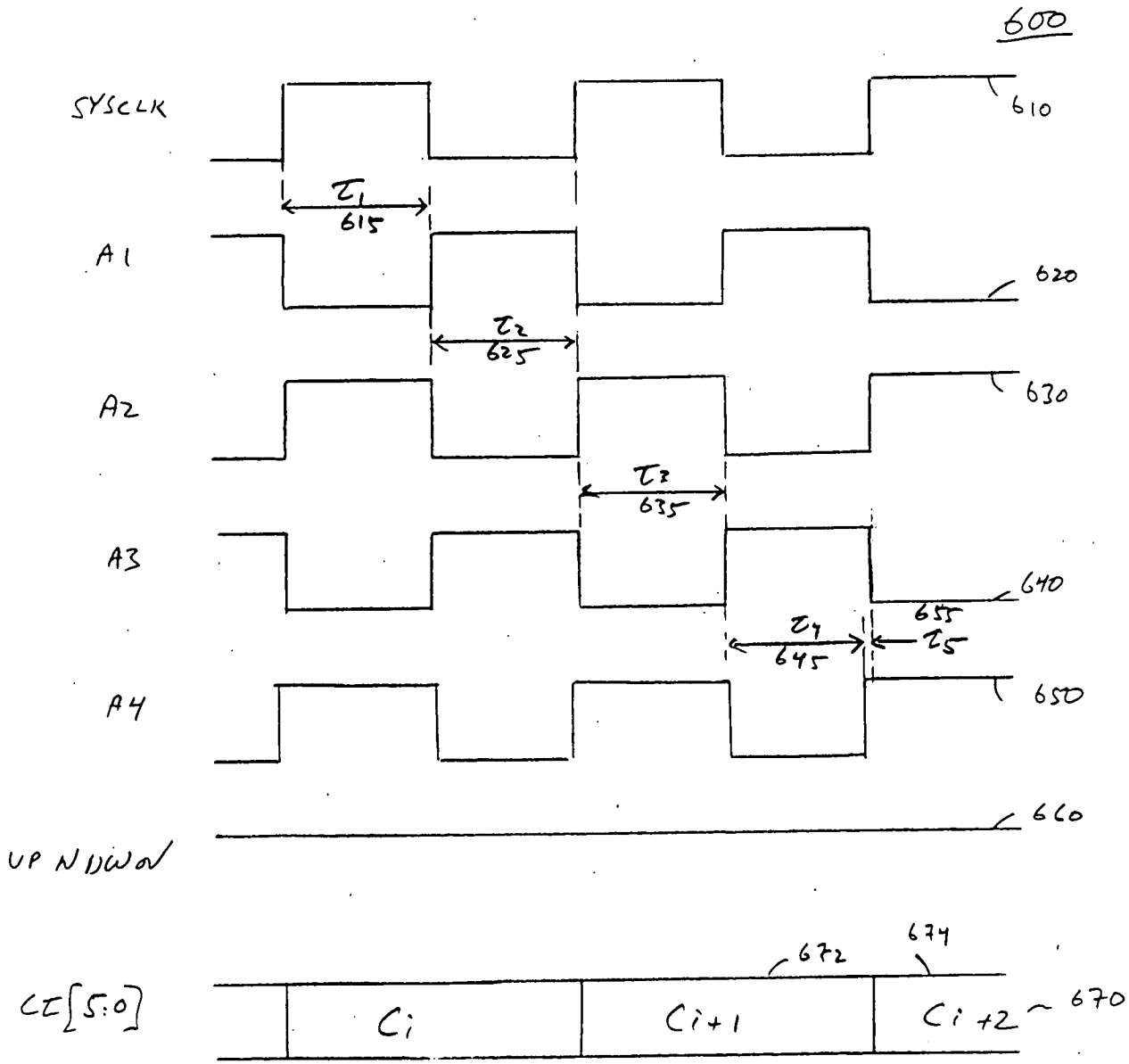
600
SYSCLK
610
τ1
615
A1
620
τ2
625
A2
630
τ3
635
A3
640
655
τ4
645
τ5
A4
650
660
UP N DOWN
672
674
CE[5:0]
Ci
Ci+1
Ci+2
670

FIGURE 6

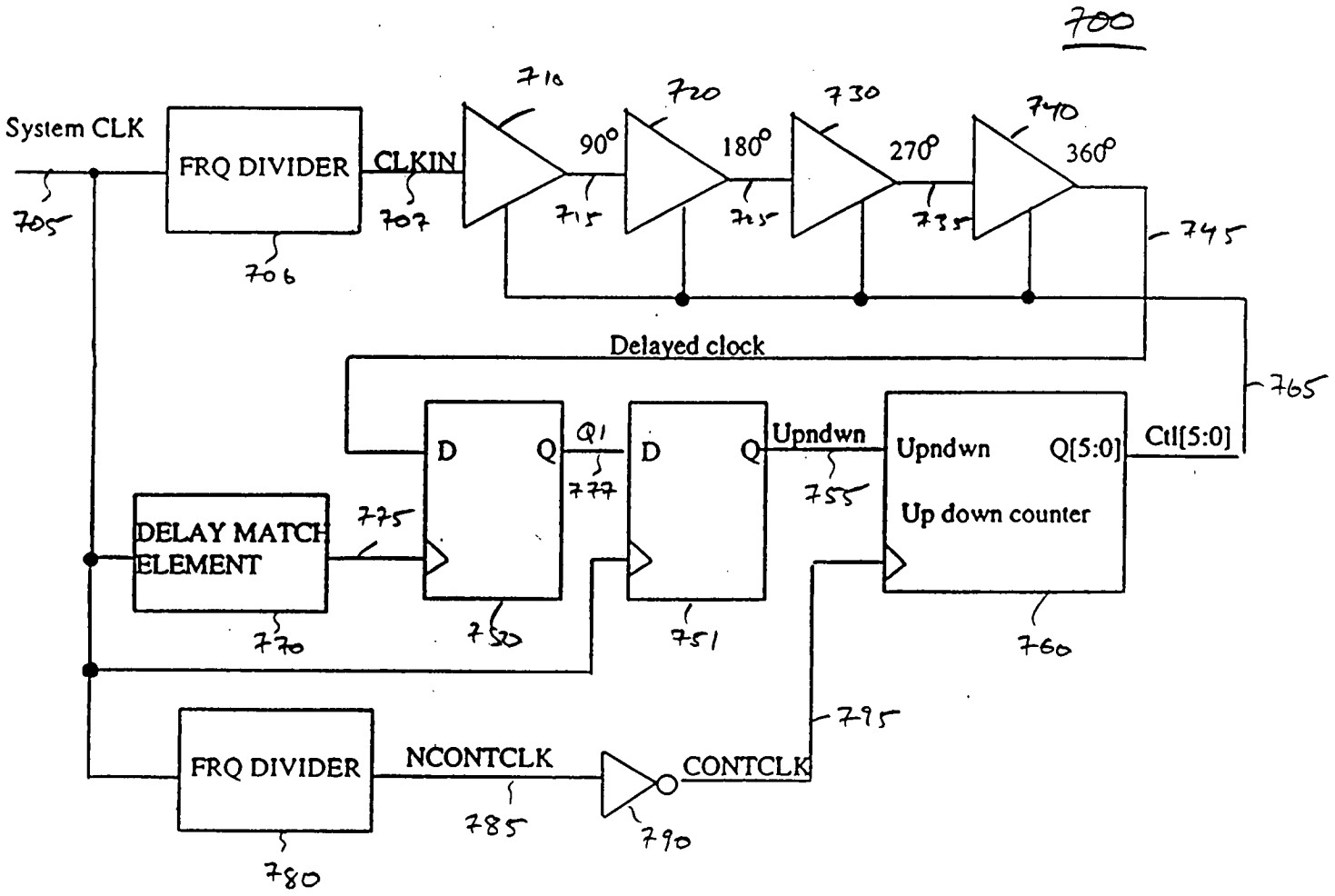
700
System CLK
FRQ DIVIDER
CLKIN
710
720
730
740
90°
180°
270°
360°
705
706
707
715
725
735
745
Delayed clock
765
D
Q
Q1
D
Q
Upndwn
Upndwn
Q[5:0]
Ctl[5:0]
Up down counter
DELAY MATCH ELEMENT
775
770
750
751
755
760
795
FRQ DIVIDER
NCONTCLK
CONTCLK
785
790
780

FIGURE 7

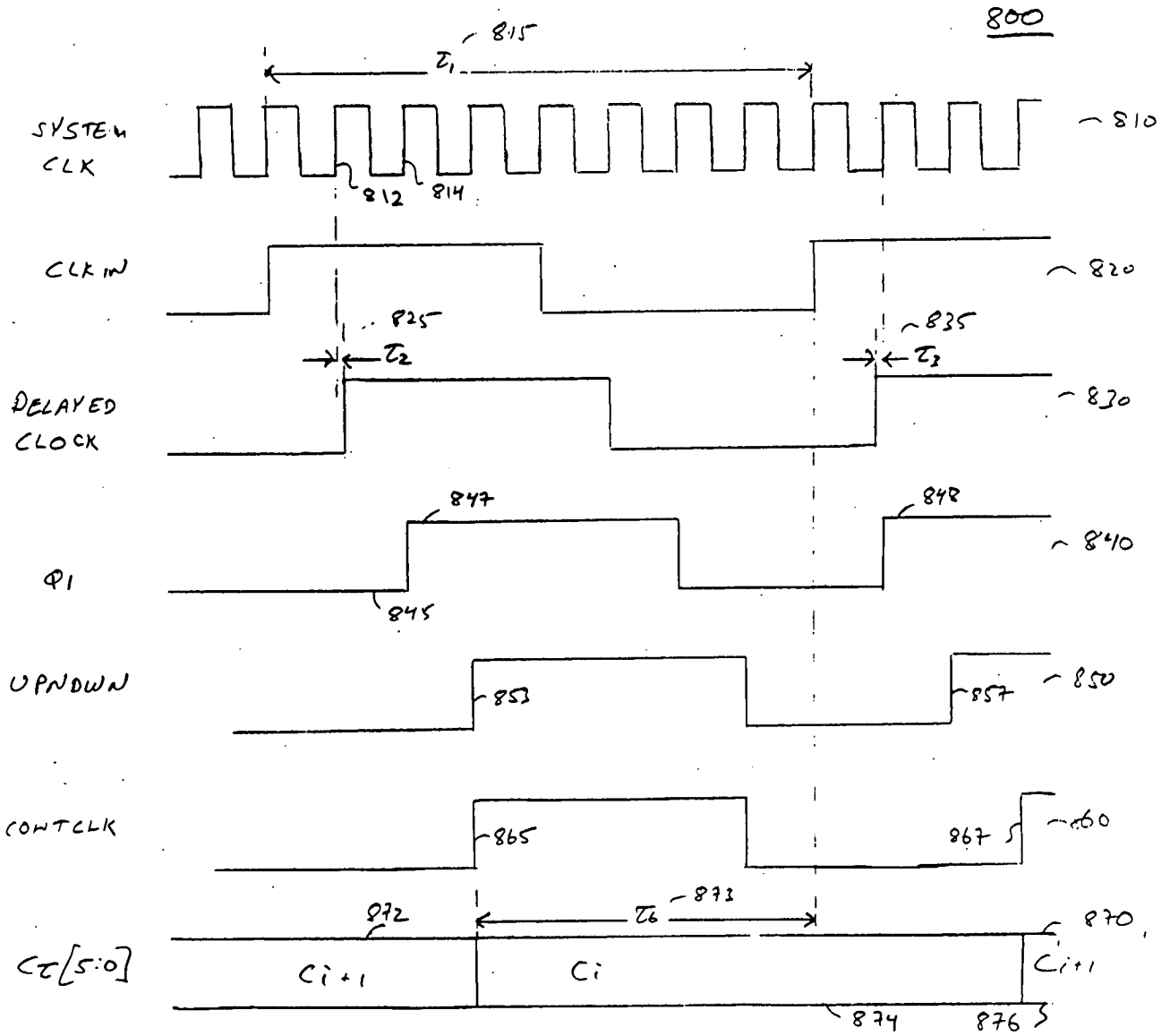
800
815
τ_1
SYSTEM CLK
810
812
814
CLK IN
820
825
835
τ_2
τ_3
DELAYED CLOCK
830
847
848
Φ_1
840
845
UPNDOWN
850
853
857
CONTCLK
860
865
867
872
τ_6
873
870
$C_T[5:0]$
C_{i+1}
C_i
C_{i+1}
874
876

FIGURE 8

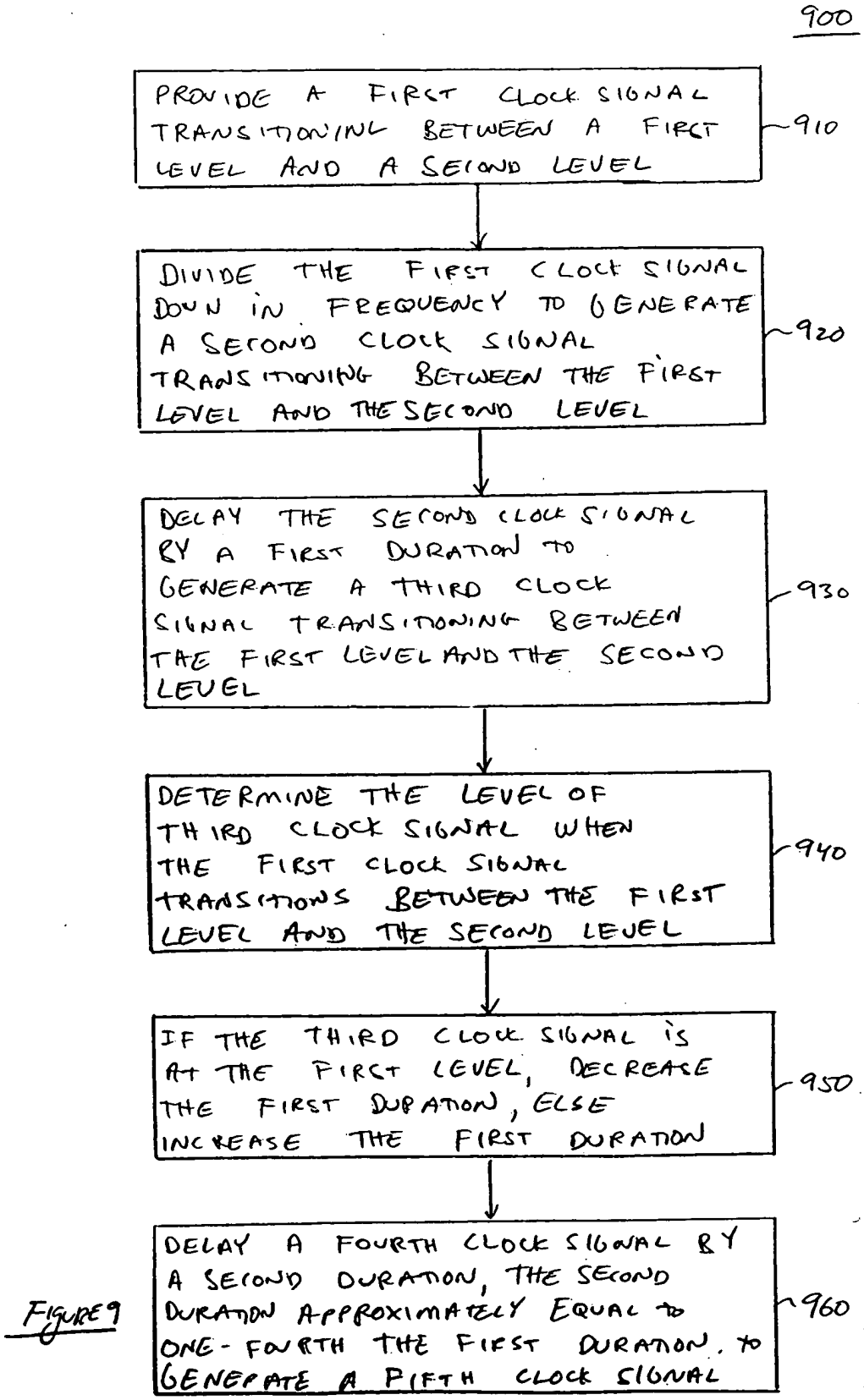
900
PROVIDE A FIRST CLOCK SIGNAL TRANSITIONING BETWEEN A FIRST LEVEL AND A SECOND LEVEL
910
DIVIDE THE FIRST CLOCK SIGNAL DOWN IN FREQUENCY TO GENERATE A SECOND CLOCK SIGNAL TRANSITIONING BETWEEN THE FIRST LEVEL AND THE SECOND LEVEL
920
DELAY THE SECOND CLOCK SIGNAL BY A FIRST DURATION TO GENERATE A THIRD CLOCK SIGNAL TRANSITIONING BETWEEN THE FIRST LEVEL AND THE SECOND LEVEL
930
DETERMINE THE LEVEL OF THIRD CLOCK SIGNAL WHEN THE FIRST CLOCK SIGNAL TRANSITIONS BETWEEN THE FIRST LEVEL AND THE SECOND LEVEL
940
IF THE THIRD CLOCK SIGNAL IS AT THE FIRST LEVEL, DECREASE THE FIRST DURATION, ELSE INCREASE THE FIRST DURATION
950
DELAY A FOURTH CLOCK SIGNAL BY A SECOND DURATION, THE SECOND DURATION APPROXIMATELY EQUAL TO ONE-FOURTH THE FIRST DURATION, TO GENERATE A FIFTH CLOCK SIGNAL
960

FIGURE 9

1000

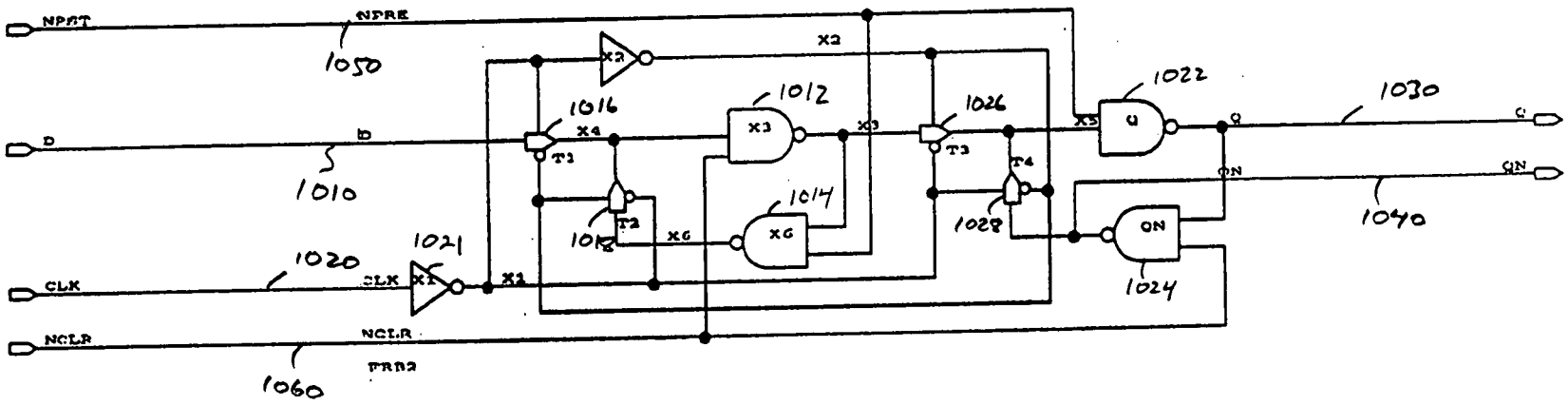

FIGURE 10

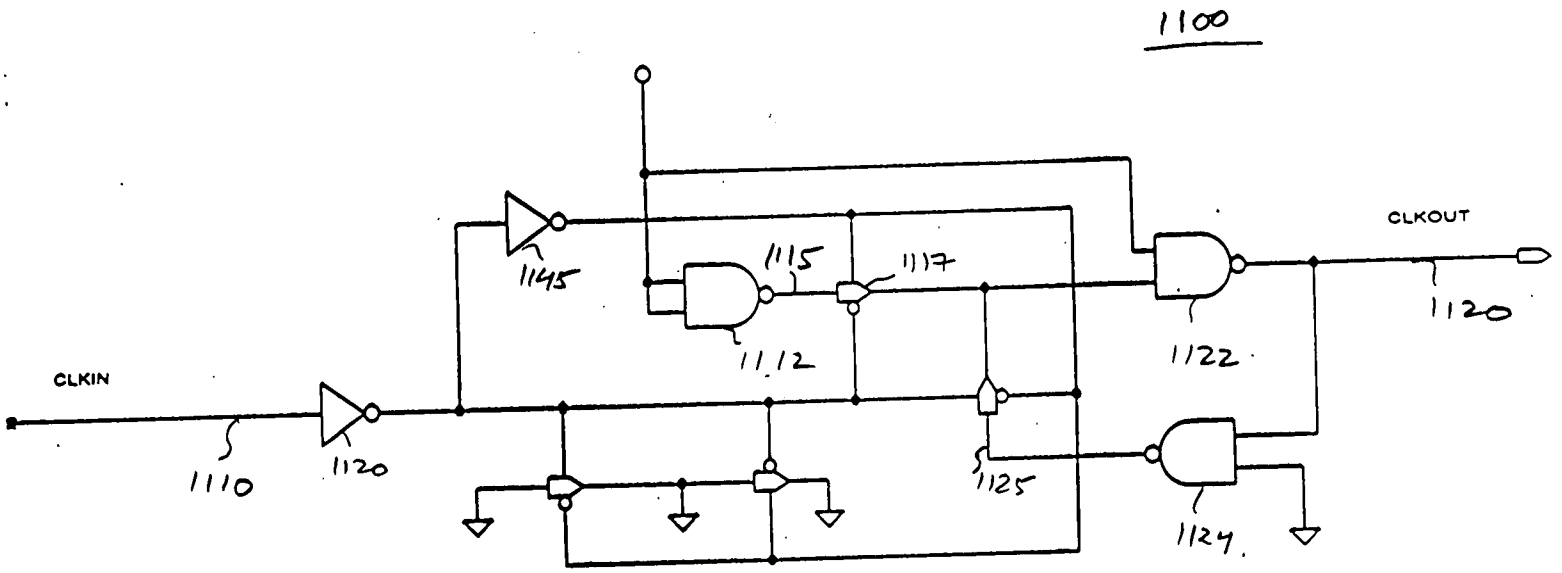
1100
CLKIN
1110
1120
1145
1115
1117
1112
1122
CLKOUT
1120
1125
1124

FIGURE 11

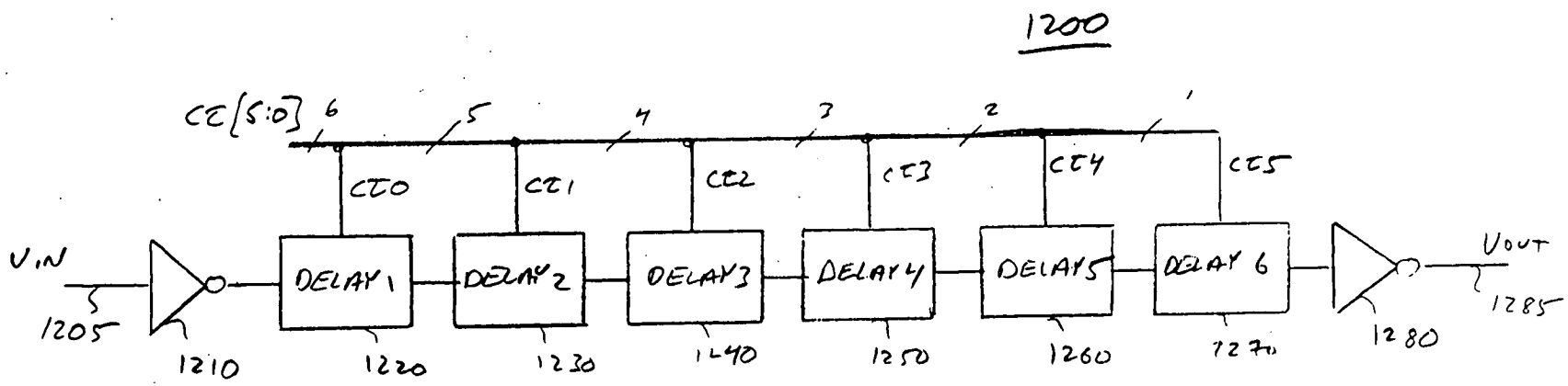
1200
CE[5:0]
6
5
4
3
2
1
CE0
CE1
CE2
CE3
CE4
CE5
VIN
1205
1210
DELAY 1
1220
DELAY 2
1230
DELAY 3
1240
DELAY 4
1250
DELAY 5
1260
DELAY 6
1270
1280
VOUT
1285

FIGURE 12

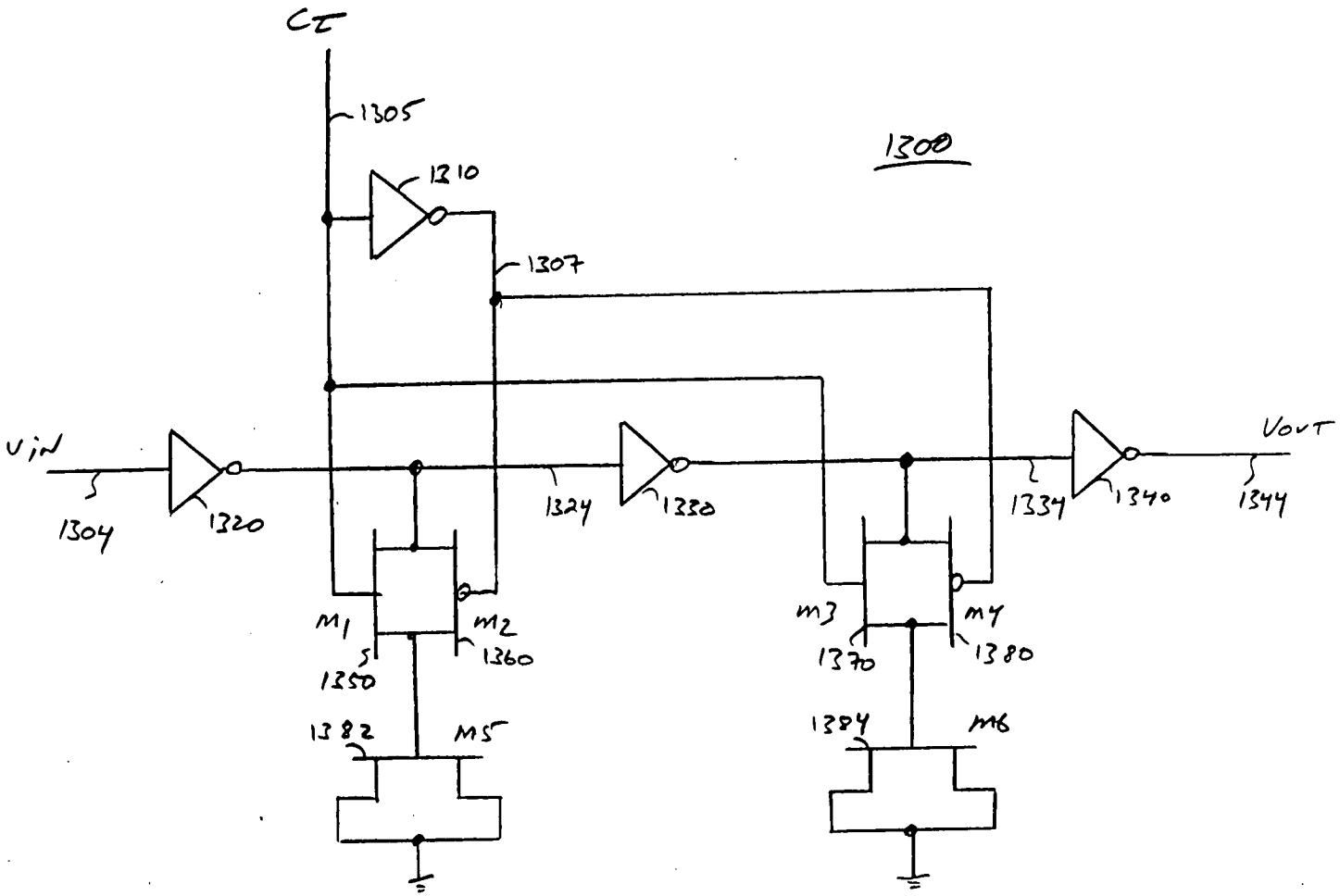
CE
1305
1300
1310
1307
Vin
1304
1320
1324
1330
1334
1340
Vout
1344
M1
M2
1350
1360
M3
M4
1370
1380
1382
M5
1384
M6

FIGURE 13

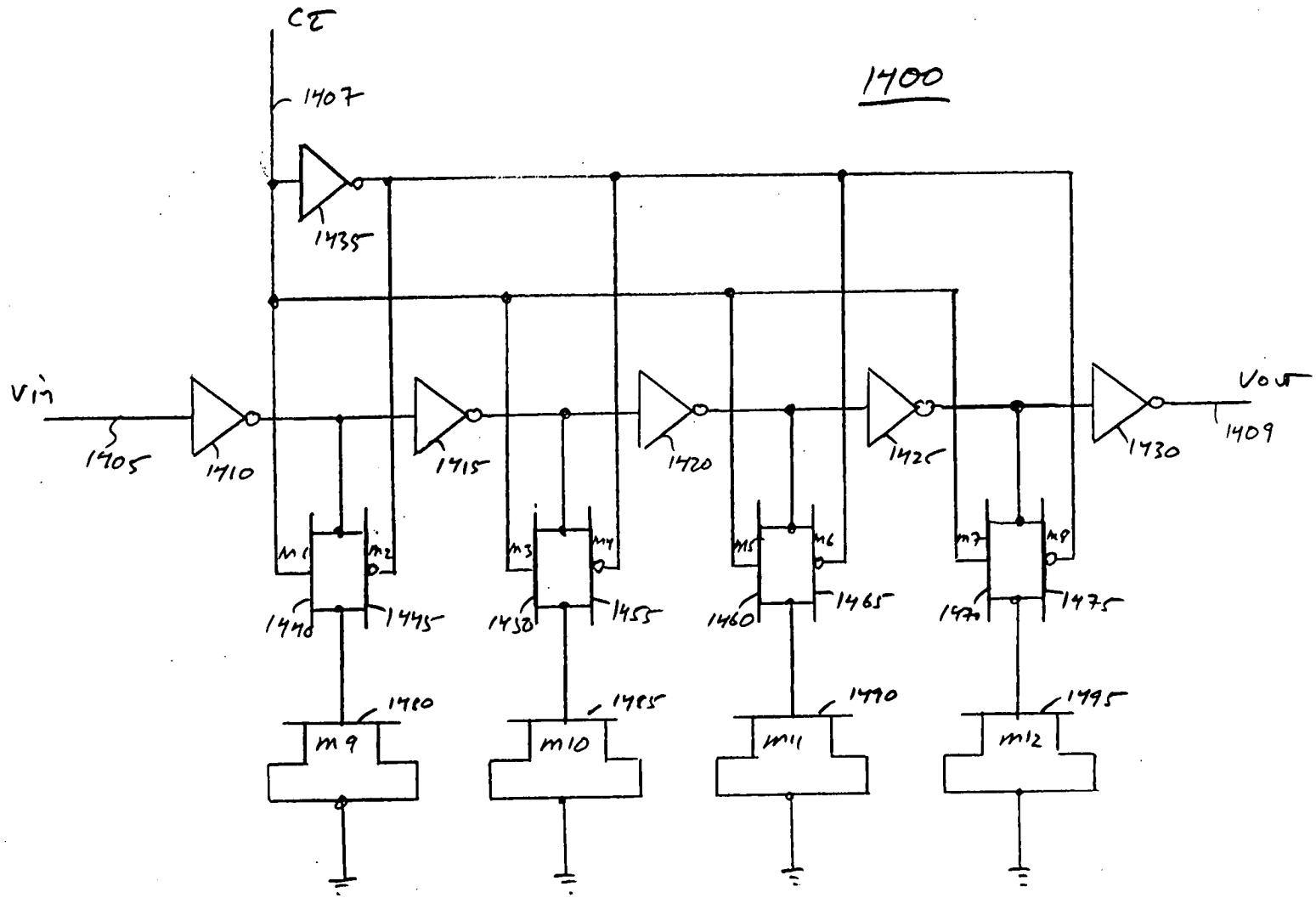
CE
1407
1400
1435
Vin
1405
1410
1415
1420
1425
1430
Vout
1409
M1
M2
M3
M4
M5
M6
M7
M8
1440
1445
1450
1455
1460
1465
1470
1475
1480
1485
1490
1495
M9
M10
M11
M12

FIGURE 14

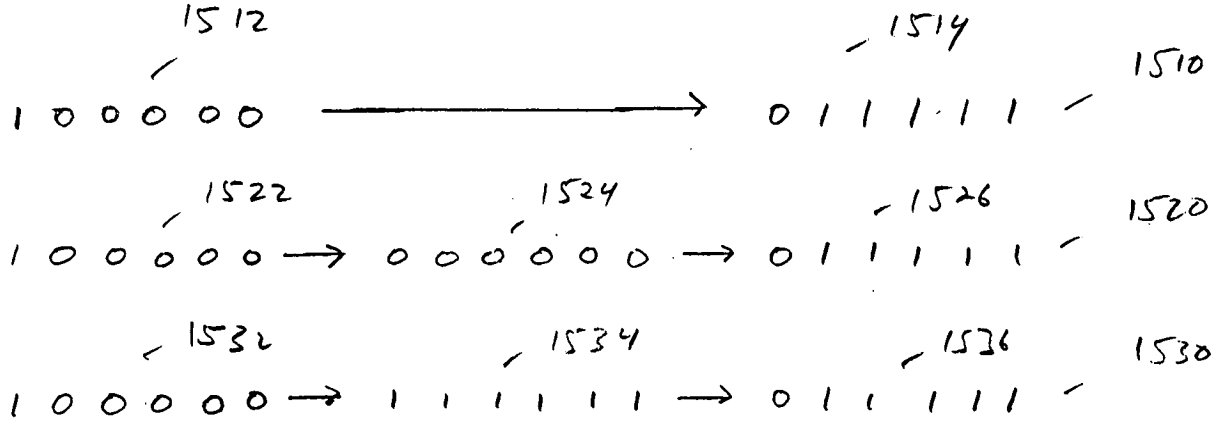
1512
1514
1510
1 0 0 0 0 0
0 1 1 1 1 1
1522
1524
1526
1520
1 0 0 0 0 0
0 0 0 0 0 0
0 1 1 1 1 1
1532
1534
1536
1530
1 0 0 0 0 0
1 1 1 1 1 1
0 1 1 1 1 1

FIGURE 15

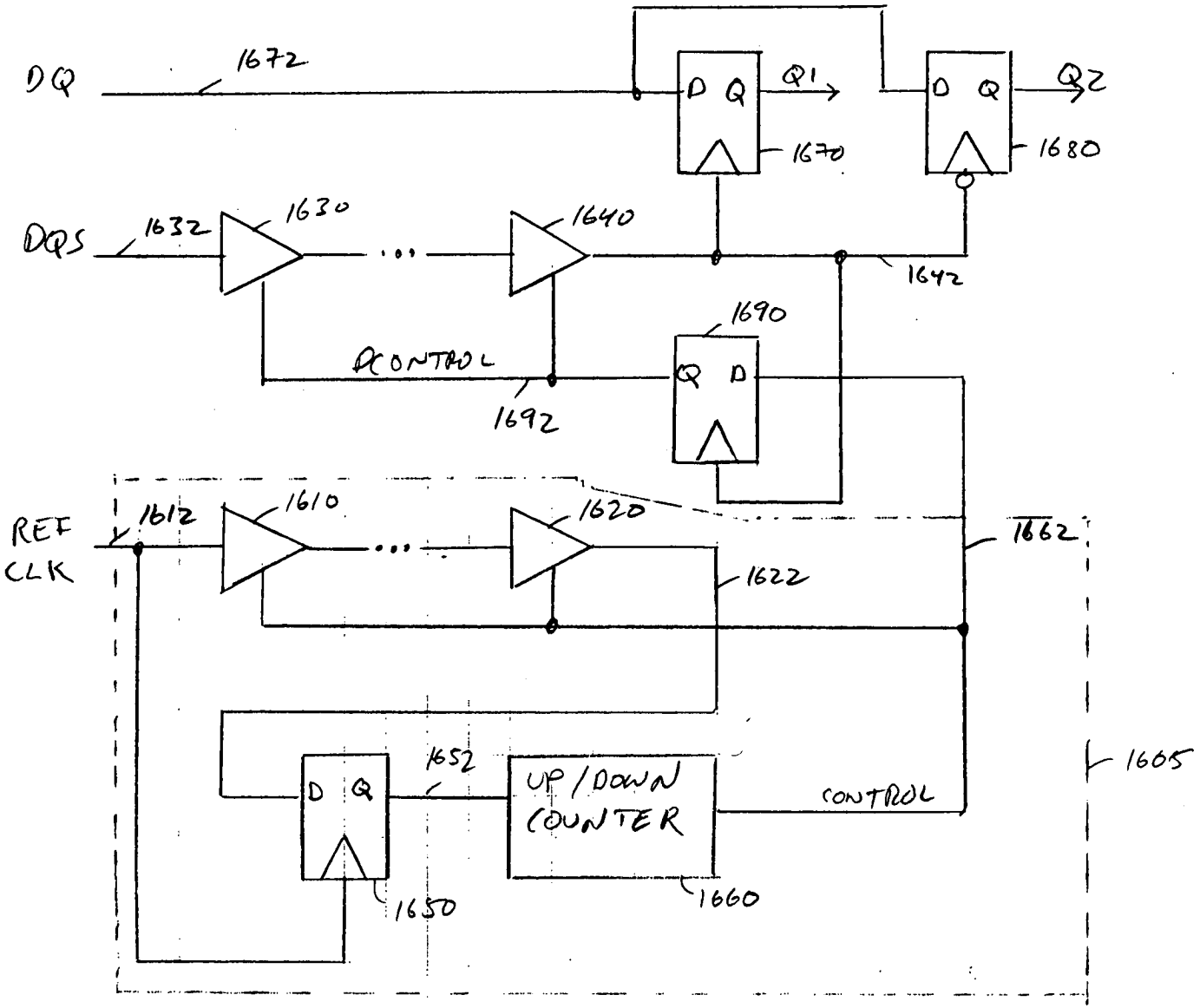
DQ
1672
D Q
Q1
1670
D Q
Q2
1680
DQS
1632
1630
1640
1642
1690
Q D
DCONTROL
1692
REF CLK
1612
1610
1620
1662
1622
1652
D Q
UP/DOWN COUNTER
CONTROL
1605
1650
1660

FIGURE 16

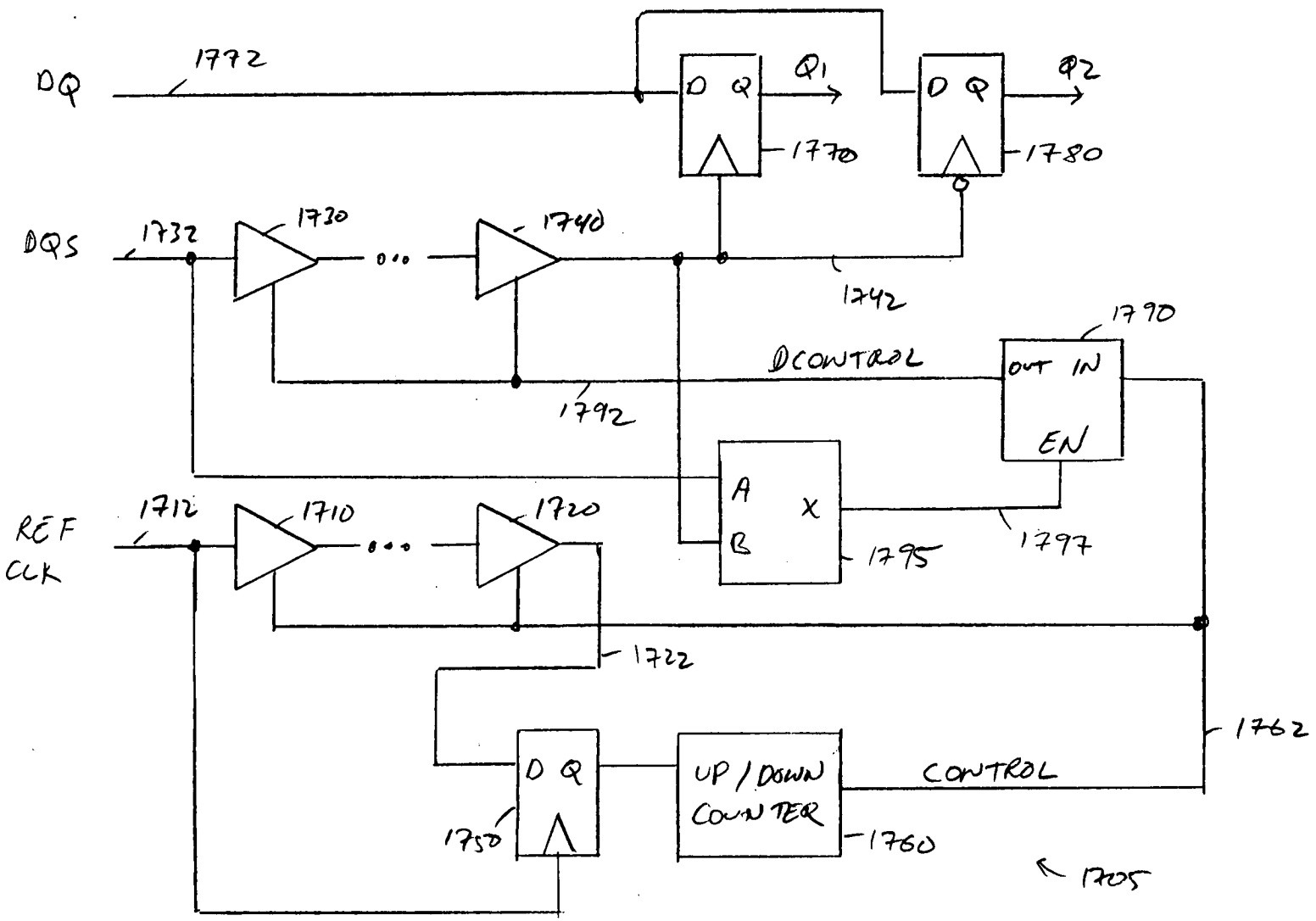
DQ
1772
D Q
Q1
1770
D Q
Q2
1780
DQS
1732
1730
1740
1742
DCONTROL
1790
OUT IN
EN
1792
A
X
B
1795
1797
REF CLK
1712
1710
1720
1722
1762
D Q
1750
UP / DOWN COUNTER
CONTROL
1760
1705

FIGURE 17

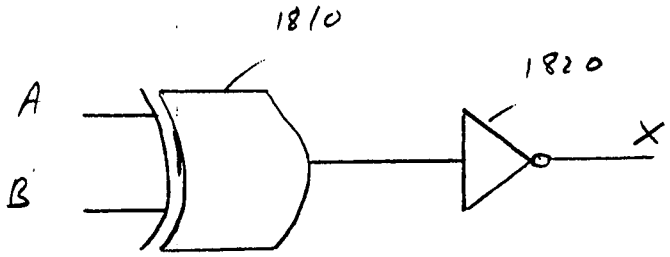

FIGURE 18

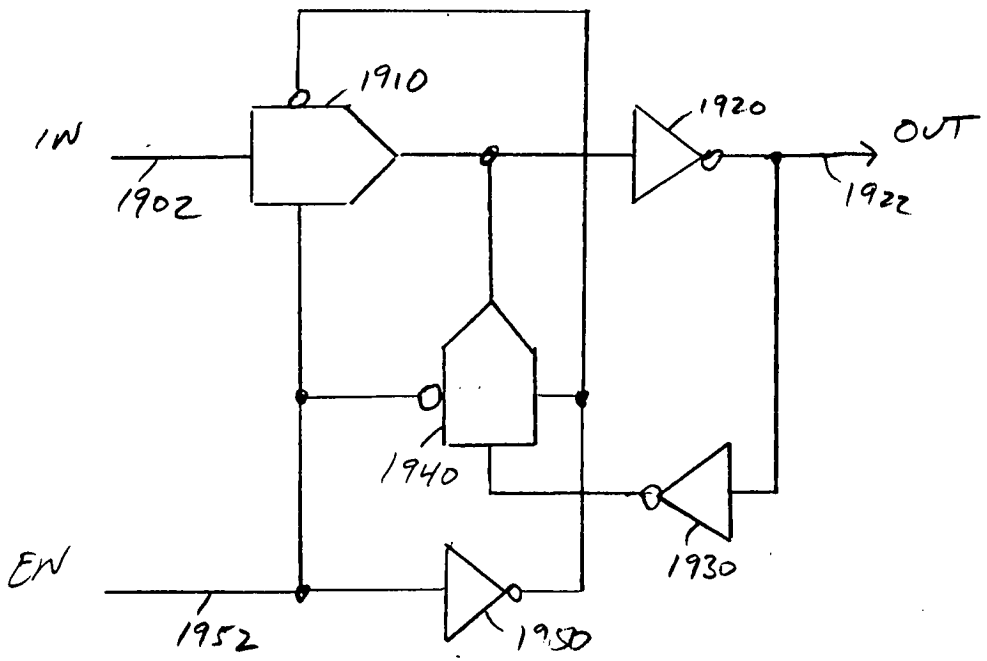

FIGURE 19

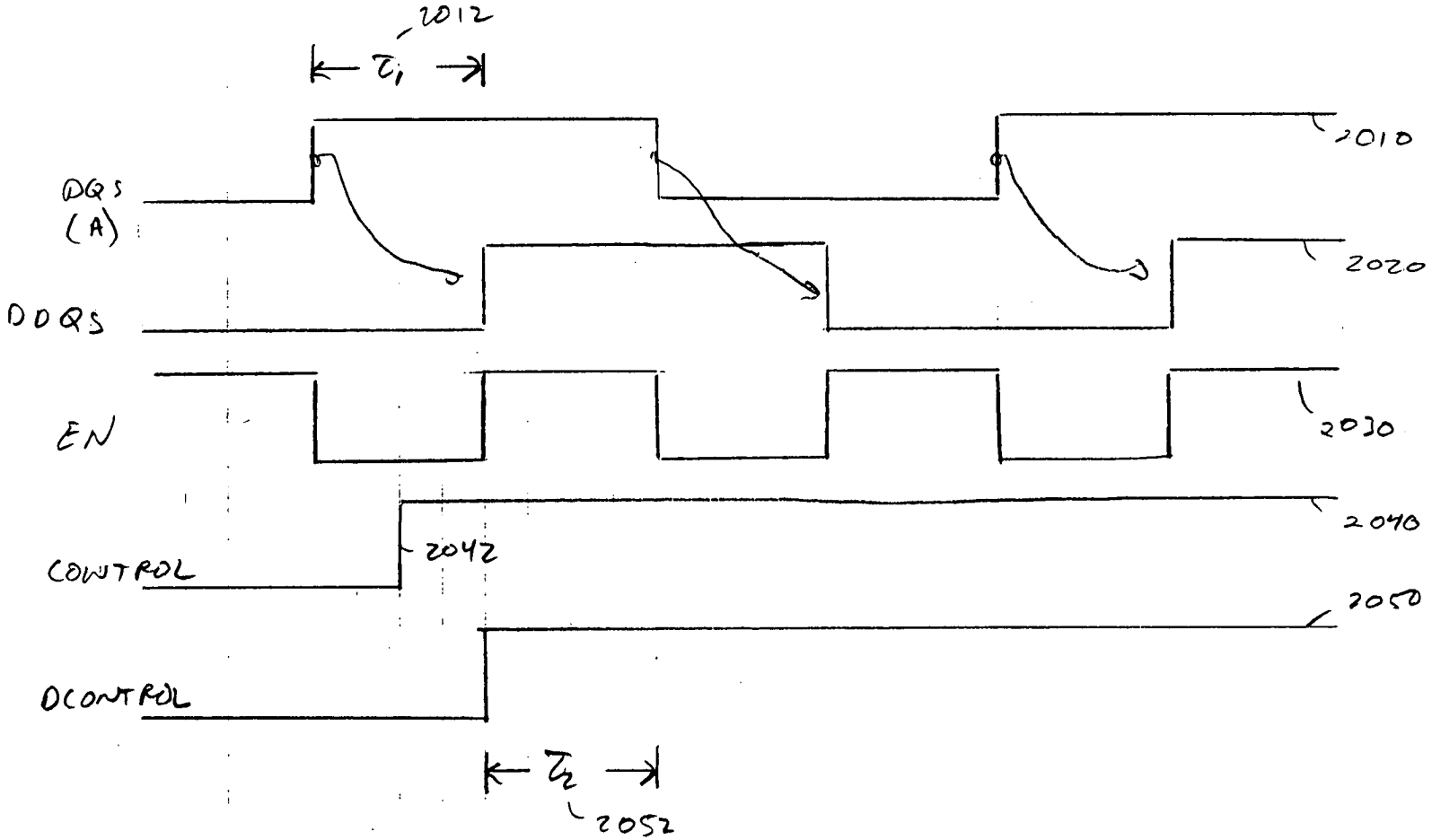
2012
τ_1
2010
DQS
(A)
2020
DDQS
EN
2030
2040
2042
CONTROL
2050
DCONTROL
τ_2
2052

FIGURE 20

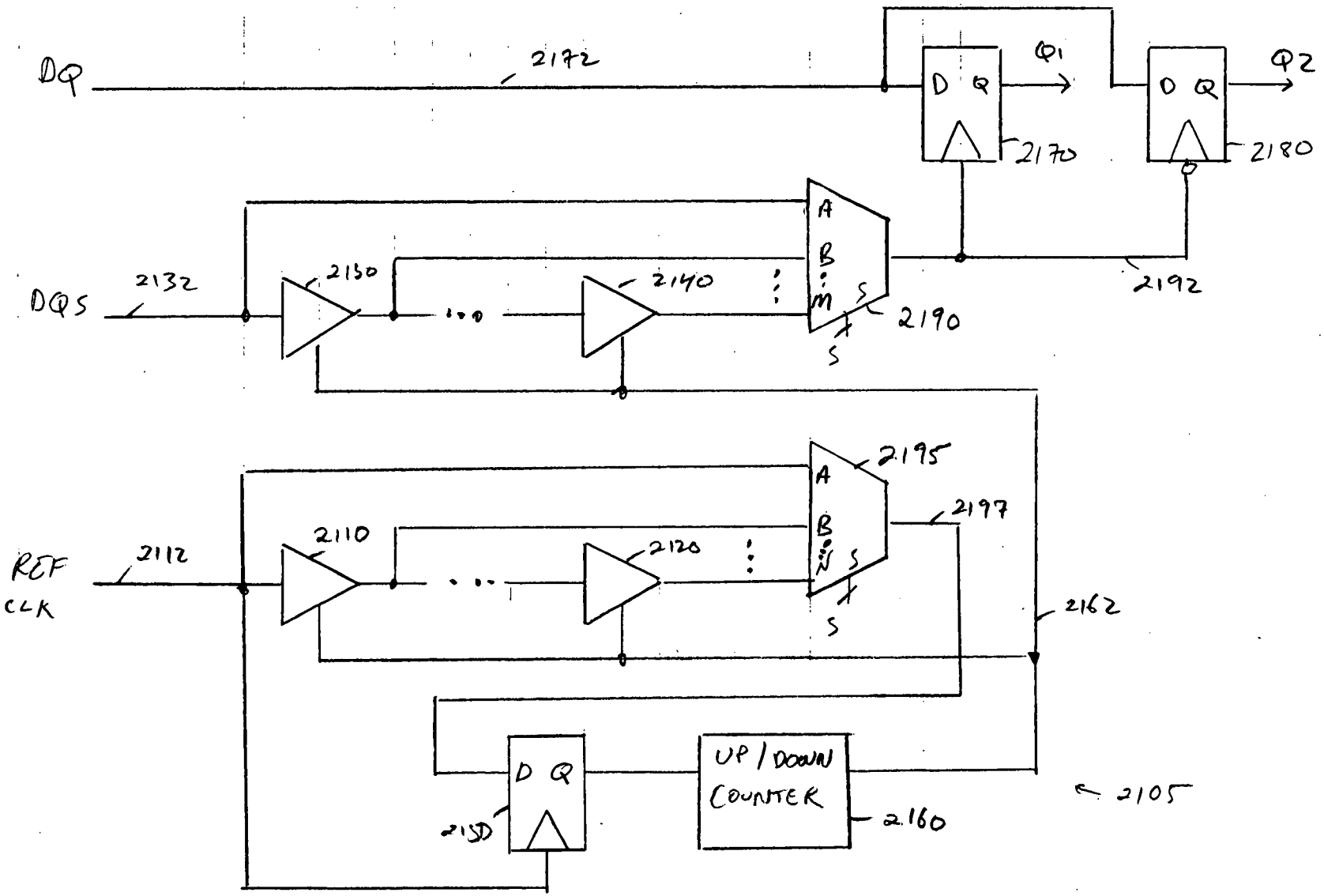
DQ
2172
D Q
Q1
2170
D Q
Q2
2180
A
B
M
S
2190
S
2192
DQS
2132
2150
2140
2195
2197
REF CLK
2112
2110
2120
N
2162
D Q
UP / DOWN COUNTER
2160
2105

FIGURE 21

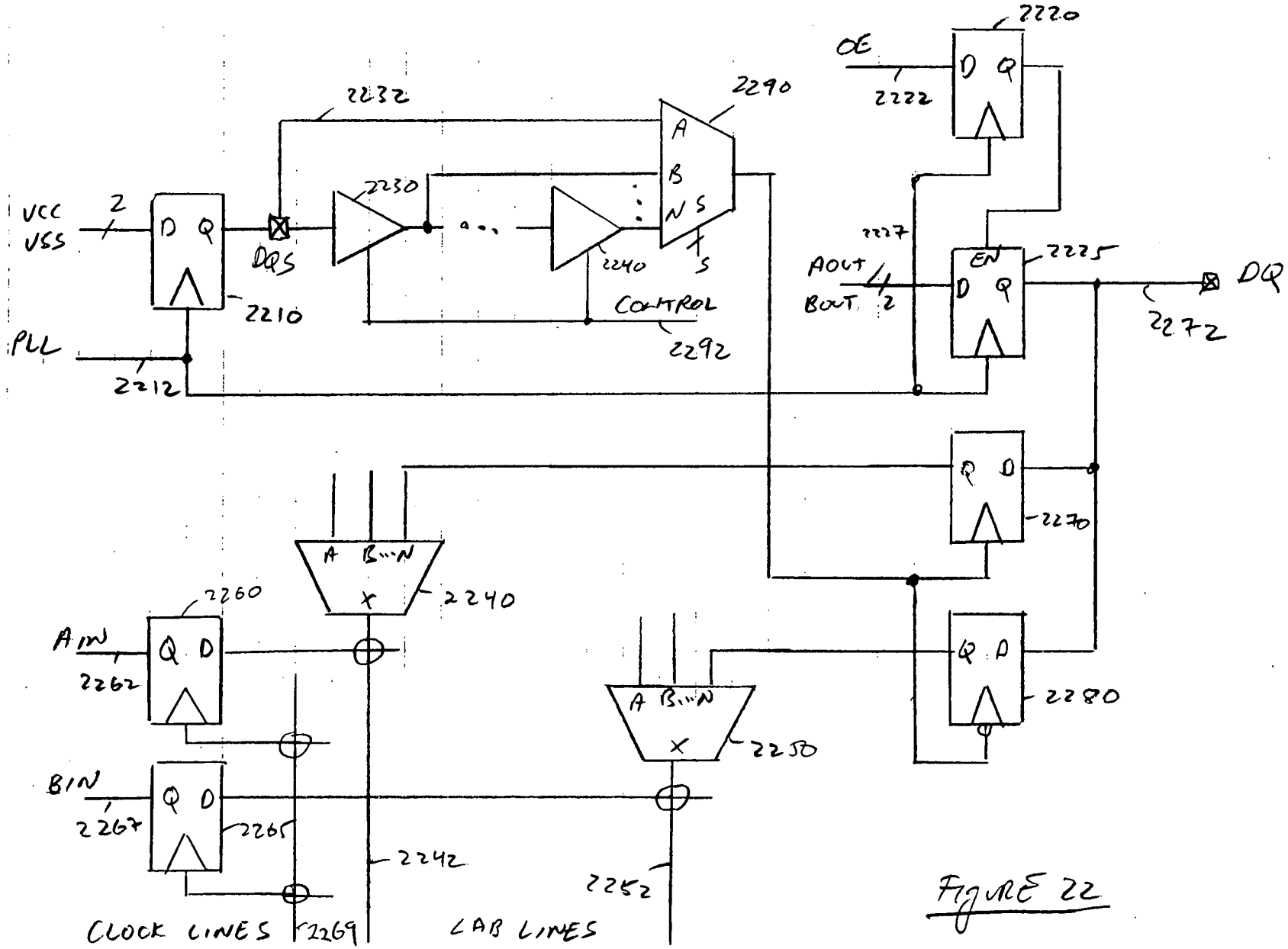
2220
OE
2222
2290
2232
A
B
N S
2230
VCC
VSS
2
D Q
DQS
2210
2240
S
CONTROL
2292
PLL
2212
2227
AOUT
BOUT 2
EN
2225
DQ
2272
Q D
2270
A B...N
X
2240
2260
AIN
2262
Q D
A B...N
X
2250
Q D
2280
BIN
2267
Q D
2265
2242
2252
CLOCK LINES 2269
LAB LINES

Figure 22

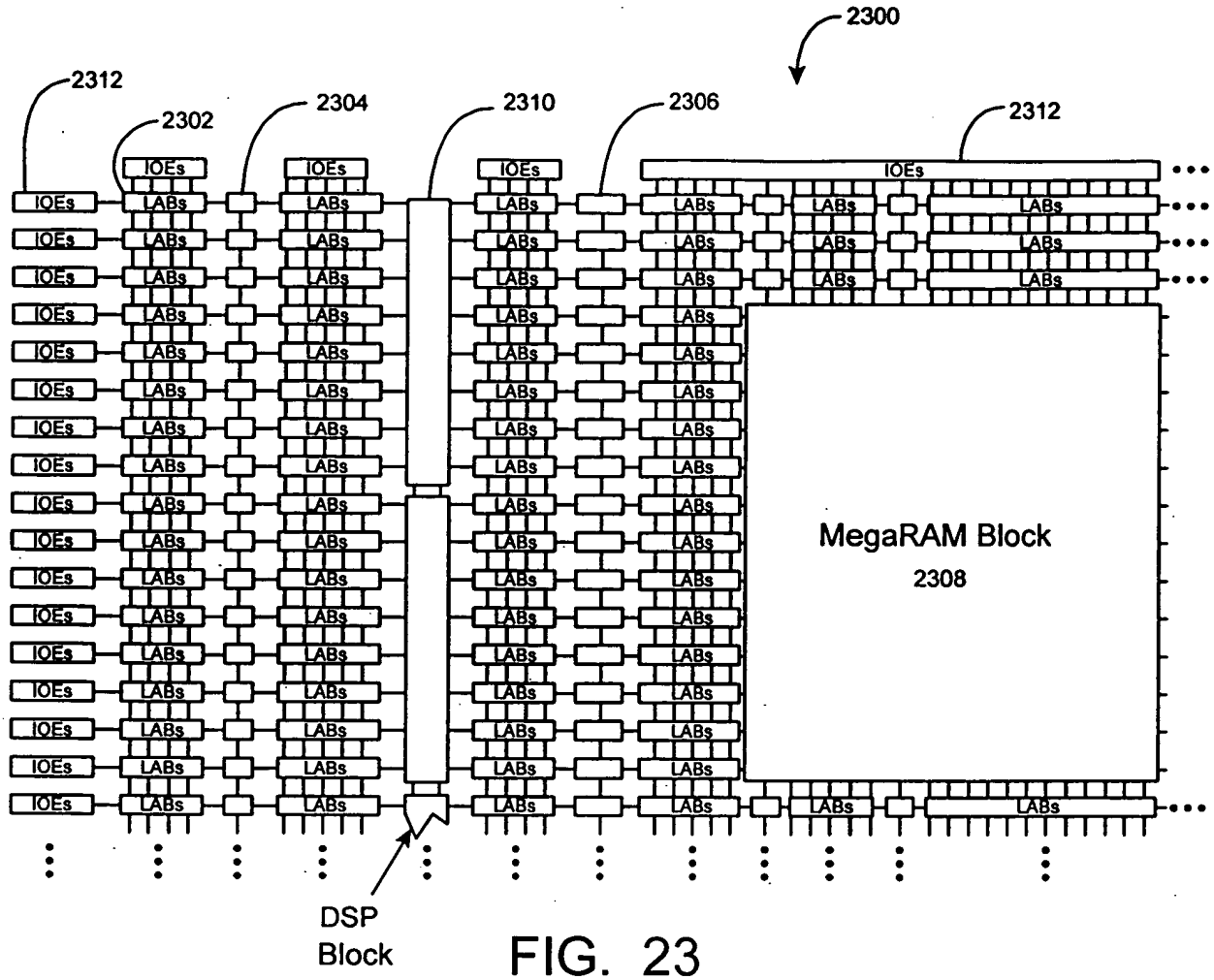
2300
2312
2302
2304
2310
2306
2312
IOEs
LABs
MegaRAM Block
2308
DSP
Block

FIG. 23

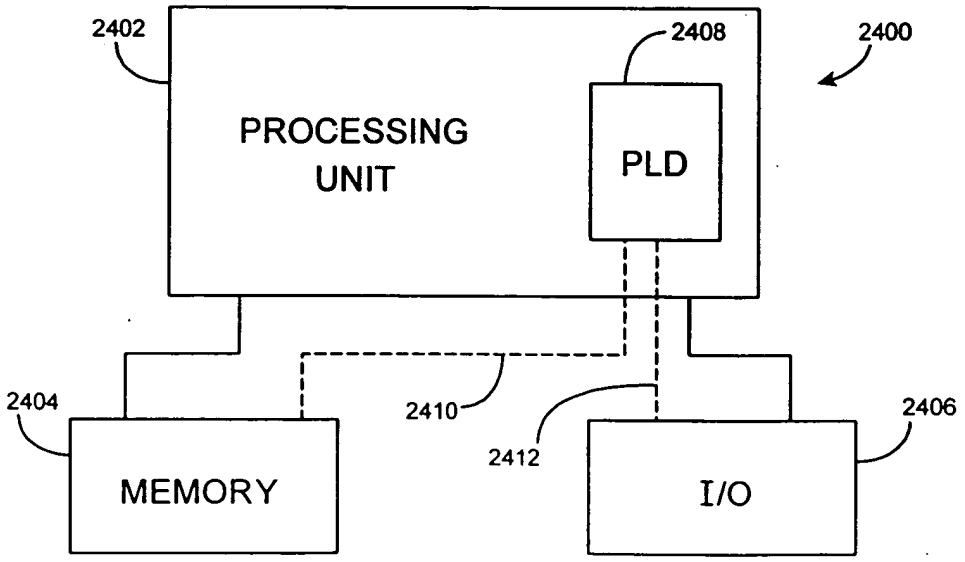
2402
2408
2400
PROCESSING
UNIT
PLD
2404
2410
2412
2406
MEMORY
I/O

FIG. 24